ECE 251: Computer Architecture
Week 05 Notes - SystemVerilog Primitives & Synchronization

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1. SystemVerilog Primitives

Primitives are the lowest-level natively supported logic gates in SV.

- **Built-in**: and, nand, or, nor, xor, xnor, not, buf.
- **Syntax**: gate_type instance_name (output, in1, in2...);
- **Tri-State**: bufif1 (passes if 1, else high-Z).
- **Delays**: Accurate physical propagation delays modeled via #(time).

User-Defined Primitives (UDPs)

Custom gate cells (like a 2:1 Mux or SR-Latch) defined entirely by Truth Tables evaluated extremely quickly by the simulator engine.

2. SystemVerilog Dataflow Assignments

Strict separation of assignment syntax is required for accurate hardware synthesis.

1. **Continuous Assignment (`assign`)**: Evaluates instantly outside procedural blocks. Acts as a continuously driven physical wire.

2. **Blocking Procedural (=)**: Evaluates strictly top-to-bottom inside `always_comb`. Used for Combinational logic.

3. **Non-Blocking Procedural (<=)**: Right-hand sides evaluate immediately, but Left-hand sides update simultaneously at the end of the step. Used exclusively inside clocked `always_ff` blocks to model Flip-Flops safely.

Warning: Never mix = and <= in the same logic block.

3. 32-Bit MIPS Addressing

MIPS instructions are rigidly 32 bits, making it impossible to encapsulate both an opcode and a 32-bit constant immediately.

- **Loading Large Constants**:
  - `lui $s0, 0xDEAD` (Load Upper Immediate)
  - `ori $s0, $s0, 0xBEEF` (OR Immediate)

- **PC-Relative Addressing**: Used by `beq`.
  - Target = `PC + 4 + (offset × 4)`. Allows rapid local jumps.

- **Register Addressing**: Used by `jr`.
  - Target = Address inside a 32-bit register. Allows absolute 4GB reach (necessary for OS kernels).

4. Hardware Synchronization & Data Races

In multicore processors, concurrent threads can corrupt shared memory if they Read-Modify-Write simultaneously (**Data Race**).

- **Atomic Operations**: Needed to build lock mechanisms without freezing the entire hardware memory bus.
- **Load Linked (**ll**)**: Reads a word and uniquely registers the memory address with the CPU.
- **Store Conditional (**sc**)**: Attempts to write back to that address. It **fails** (returns 0) if any other core modified the data since the ll. Otherwise, it succeeds (returns 1).