ECE 251: Computer Architecture

Week 04 Notes - MIPS Emulation & Intro to SystemVerilog

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1. MIPS ISA Review

1. **Simplicity favors regularity**: Fixed instruction sizes (32 bits).
2. **Smaller is faster**: Limited register file (32 general purpose registers).
3. **Make the common case fast**: Optimize arithmetic and data movement.
4. **Good design demands good compromises**: E.g., introducing the limited I-Type format to handle immediate constants efficiently.

Load/Store Architecture

MIPS inherently prohibits direct memory-to-memory operations. Data MUST be **loaded** into a register, manipulated, and then **stored** back to RAM.

2. The Supervisor & Emulation

A physical CPU typically runs an Operating System to manage programs. For MIPS, we use simulators like **SPIM** or **MARS**.

- **Loading**: Placing instructions into the Text Segment (`0x00400000`) and statics into the Data Segment (`0x10000000`).
- **Execution**: Managing the Program Counter (`PC`).
- **System Calls (`syscall`)**: Handing execution back to the emulator to perform restricted OS-level functions:
  - Consuming input or printing to the terminal.
  - Halting execution cleanly (Exit).

3. Case Study: Quake's Fast Inverse Square Root

The legendary algorithm used in *Quake III Arena* (1999) to compute $\frac{1}{\sqrt{x}}$ for 3D lighting without expensive division circuitry.

```
# i  = 0x5f3759df - ( i >> 1 );
mfc1  $t0, $f12          # Move float to integer register (Bit Hack)
srl   $t1, $t0, 1        # i >> 1 (Logical shift right)
lw    $t2, magic         # Load magic number (0x5f3759df)
sub   $t0, $t2, $t1      # Subtract to get initial guess
mtc1  $t0, $f0           # Move bits back to float register
```

- **The Magic**: Exploits the IEEE 754 log-based exponent representation to rapidly approximate $x^{-0.5}$.

4. Introduction to SystemVerilog (SV)

SystemVerilog is a Hardware Description Language (HDL) used to design structured, parallel digital circuits.

- **Compilation**: We use `iverilog` to aggressively synthesize models.
- **Simulation**: We use `vvp` as the runtime engine.
- **Waveforms**: Visualization generated by `GTKWave`.

Data Types vs Software

A `logic` variable models a physical wire. It isn't just an integer; it enforces a strict rule against multiple short-circuiting electrical drivers.

5. Logic Modeling Paradigms in SV

- **Structural**: Instantiating physical logic primitives natively (e.g., `and`, `or`, `not`) and cabling them explicitly. Best for explicit delay modeling.
- **Dataflow**: Highly preferred continuous assignment (`assign`) using Boolean operators (`&`, `|`, `^`). The compiler optimizes the final gate netlist.

- **Combinational Logic**: Output intimately depends *only* on present inputs. Designed via `assign` or `always_comb`.
- **Sequential Logic**: Employs memory buffers reliant on historical state and a synchronous *Clock*. Designed via `always_ff`.